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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				<i>Complete if Known</i>	
				Application Number	
				Filing Date	
				First Named Inventor	
				Group Art Unit	
				Examiner Name	
				Attorney Docket Number	
Sheet	1	of	3	Marius K. Orlowski	
				SC12885TP	

U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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Examiner Signature	<i>Pr. Review</i>	Date Considered	02/27/05
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Signature: W. R. ... Considered: ...

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Sheet	2	of	3	Attorney Docket Number	SC12885TP

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
BK	AH	MONFRAY, S. et al.; "50nm-Gate All Around (GAA)-Silicon On Nothing (SON)-Devices: A Simple Way to Co-Integration of GAA Transistors Within Bulk MOSFET Process"; 2002 Symposium on VLSI Technology; 2002; pp 108-109; 2002 Symposium on VLSI Technology Digest of Technical Papers	
BK	AI	MONFRAY, S. et al.; "Highly-Performant 38nm SON (Silicon-On-Nothing) P-MOSFETs with 9nm-thick Channels"; 2002 IEEE International SOI Conference; 10/02; pp 20-22	
BK	AJ	MONFRAY, S. et al.; "SON (Silicon-On-Nothing) P-MOSFETs with Totally Silicided (CoSi ₂) Polysilicon on 5nm-thick Si Films: The Simplest Way to Integration of Metal Gates on Thin FD Channels"; IEDM; 2002; pp 263-266; IEEE	
BK	AK	YU, Bin et al; "FinFET Scaling to 10nm Gate Length"; IEDM; 2002; pp 251-254; IEEE	
BK	AL	KEDZIERSKI, Jakub et al.; "High Performance Symmetric-Gate and CMOS-Compatible V _t Asymmetric-Gate FinFET Devices"; IEEE; 2001; 4 pp	
BK	AM	CHOI, Y. et al.; "Sub-20nm CMOS FinFET Technologies"; IEDM; 2001; pp 19.1.1-19.1.4; IEEE	
BK	AN	KIM, K. et al.; "Double-Gate CMOS: Symmetrical-Versus Asymmetrical-Gate Devices"; IEEE Transactions on Electron Devices; February, 2001; pp 294-299; Vol 48, No 2; IEEE	
BK	AO	MONFRAY, S. et al.; "First 80nm SON (Silicon-On-Nothing) MOSFETs With Perfect Morphology and High Electrical Performance"; IEDM; 2001; pp 29.7.1-29.7.4; IEEE	
BK	AP	HISAMOTO, D. et al.; "FinFET-A Self-Aligned Double-Gate (MOSFET) Scalable to 20nm"; IEEE Transactions of Electron Devices; December 2000; pp 2320-2325; Vol 47, No 12; IEEE	

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BE	AQ	JURCZAK, M. et al.; "Silicon-on-Nothing (SON) - an Innovative Process for Advanced CMOS"; IEEE Transactions on Electron Devices; November, 2000; pp 2179-2187; Vol 47, No 11; IEEE	
BE	AR	FOSSUM, J.G. et al.; "Extraordinarily High Drive Currents in Asymmetrical Double-Gate MOSFETs"; Superlattices and Microstructures; 2000; pp 525-530; Vol 28; No 5/6; Academic Press	
BE	AS	JURCZAK, M. et al.; "SON (Silicon on Nothing) - A New Device Architecture for the ULSI Era"; Symposium of VLSI Technology Digest of Technical Papers; 1999; pp 29-30	
BE	AT	HUANG, X. et al.; "Sub 50-nm FinFET: PMOS"; IEDM; 1999; pp 3.4.1-3.4.4; IEEE	
BE	AU	HISAMOTO, D. et al.; "A Folded-Channel MOSFET for Deep-sub-tenth Micron Era"; IEDM; 1998; pp 1032-1034; IEDM	
BE	AV	TANAKA, T. et al.; "Ultrafast Operation of V_{th} -Adjusted p^+-n^+ Double-Gate SOI MOSFET's"; IEEE Electron Device Letters; October 1994; pp 386-388; Vol 15, No 10; IEEE	
BE	AW	International Search Report	
BE	AX	Specification, abstract and drawings for Application No. 10/074,732 Filed February 13, 2002	

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